



100V, 57A, 17.6mΩ N-channel Power SGT MOSFET

JMSL1018PGQ

Features

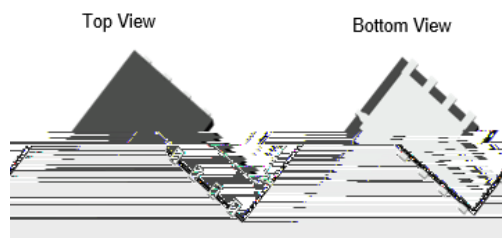
Ultra-low ON-resistance, $R_{DS(ON)}$
Low Gate Charge
100% UIS Tested
100% V_{DS} Tested
Halogen-free; RoHS-compliant
AEC-Q101 Qualified

Applications

Load Switch
PWM Application
General Automotive Application

Product Summary

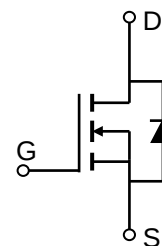
Parameters	Value	Unit
V_{DSS}	100	V
$V_{GS(th)}_{Typ}$	1.5	V
$I_D(@V_{GS}=10V)$	57	A
$R_{DS(ON)}_{Typ}(@V_{GS}=10V)$	13.2	mΩ
$R_{DS(ON)}_{Typ}(@V_{GS}=4.5V)$	17.6	mΩ



PDFN5x6-8L



Pin Assignment



Schematic Diagram

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMSL1018PGQ-13	L1018PQ	1	Tape&Reel	PDFN5x6-8L	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

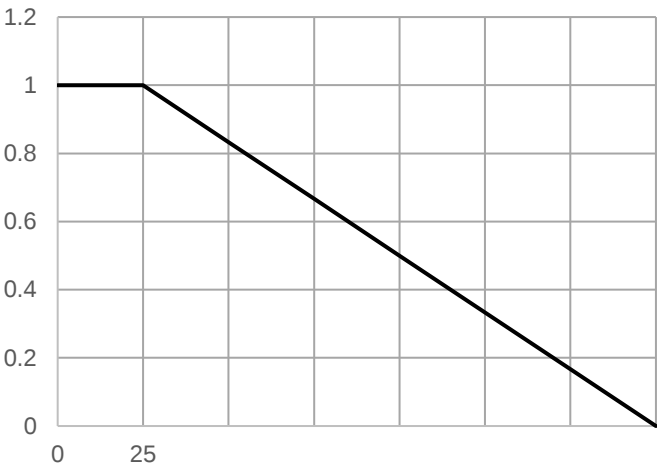
Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$: 57 $T_C = 100^\circ\text{C}$: 41	A
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	44	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$: 105 $T_C = 100^\circ\text{C}$: 52	W
$T_{J \text{ STG}}$	Junction & Storage Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Max	Unit
R	Thermal Resistance, Junction to Ambient ⁽³⁾	46	$^\circ\text{C/W}$
R	Thermal Resistance, Junction to Case	1.4	



Typical Performance Characteristics



Typical Performance Characteristics

Test Circuit

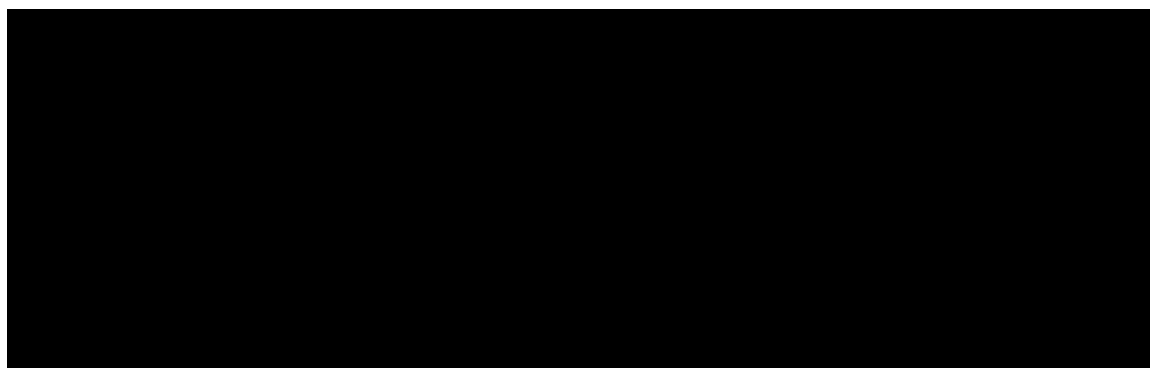


Figure 1: Gate Charge Test Circuit & Waveform

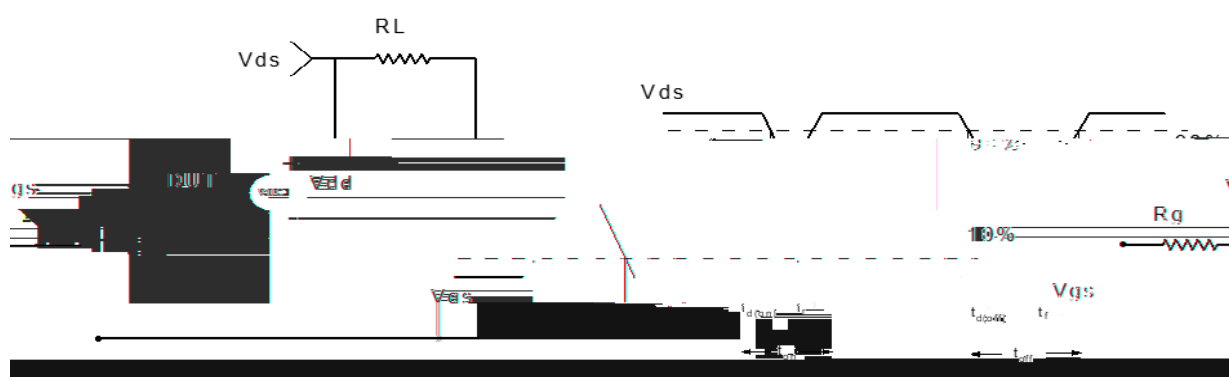


Figure 2: Resistive Switching Test Circuit & Waveform

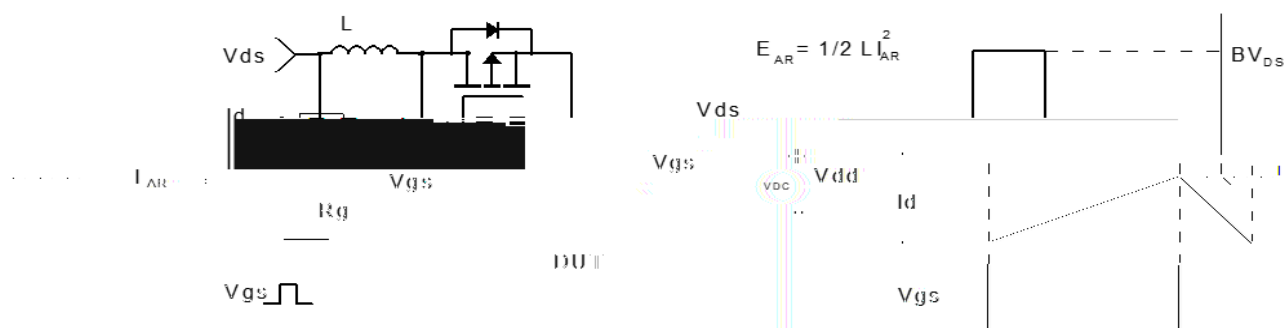


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

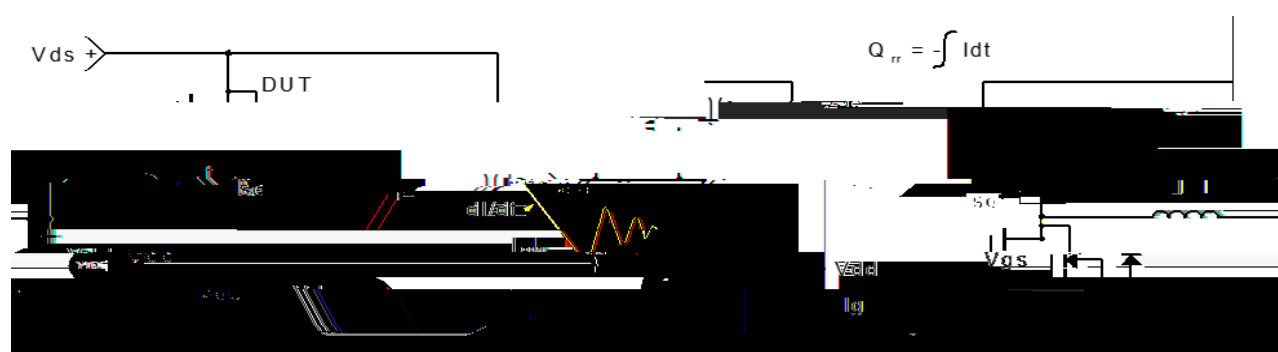
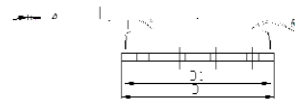


Figure 4: Diode Recovery Test Circuit & Waveform



Package Outline



Front View

NOTES

- | MILLIMETER | | |
|------------|------|------|
| L | NOM. | MAX. |
| 9 | 1 | 1.15 |

DIM.	M.
A	C

Figure 1: Schematic diagram of the experimental setup. The diagram shows a top-down view of a rectangular arena with a central platform. The arena is divided into four quadrants by a vertical dashed line and a horizontal dashed line. The central platform is labeled '4.300'. The four quadrants are labeled '0.610', '1.230', '1.850', and '2.470'. The arena is surrounded by a black border. The diagram is labeled 'Figure 1' at the bottom.



is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.

